CLAIMS

What is claimed is:

1. A flash memory, comprising:

a substrate;

a wordline formed on said substrate having, on a first side, a first sidewall having a first slope angle with respect to said substrate, and, on a second side, a second sidewall having a second slope angle greater than said first slope angle; and

at least one floating gate selectively formed on said second sidewall of the wordline, wherein said at least one floating gate is surrounded on a plurality of sides by said second sidewall.

2. The flash memory according to claim 1, wherein said at least one floating gate is selectively formed on only said second sidewall of the wordline, and said substrate comprises silicon, and

wherein adjacent ones of said at least one floating gate are isolated from each other and said second sidewall includes tapered regions provided between the adjacent ones of said at least one floating gate.

3. The flash memory according to claim 1, wherein said at least one floating gate includes at least two sides surrounded by said second sidewall.

4. The flash memory according to claim 3, wherein said at least one floating gate includes three sides surrounded by said second sidewall.

5. A memory, comprising:

a gate conductor having first and second sides, said first side having a slope and said second side having a substantially vertical wall prior to

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deposition of a polysilicon spacer material; and

at least one floating gate formed of said polysilicon spacer material and formed on said second side of said gate conductor such that said gate conductor surrounds said at least one floating gate on a plurality of sides.

6. The memory according to claim 5, wherein said gate conductor is formed on a silicon substrate, and

wherein adjacent ones of said at least one floating gate are isolated from each other and said second sidewall includes tapered regions provided between the adjacent ones of said at least one floating gate.

7. The memory according to claim 5, wherein said gate conductor surrounds said at least one floating gate on only two sides.

8. The memory according to claim 5, wherein said gate conductor surrounds said at least one floating gate on at least two sides.

9. The memory according to claim 8, wherein said gate conductor surrounds said at least one floating gate on three sides.

10. The memory according to claim 5, wherein said at least one floating gate is self-isolated from an adjacent floating gate by said gate conductor.

11. The memory according to claim 10, wherein said gate conductor surrounds said at least one floating gate on at least two sides.

12. A method of forming a flash memory, comprising steps of:

forming a polysilicon wordline on a substrate, said wordline having first and second sidewalls, said first sidewall being tapered, with respect to a surface of said substrate, to have a first slope angle, and said second

sidewall having a second slope angle greater than said first slope angle; and

forming a polysilicon spacer as a floating gate of said flash memory on said second sidewall, while simultaneously removing polysilicon on the first sidewall, said floating gate being surrounded on at least two sides thereof by said second sidewall.

13. The method according to claim 12, wherein said step of forming the polysilicon spacer as the floating gate includes using a phase-shift mask.

14. The method according to claim 12, wherein said step of forming the polysilicon spacer as the floating gate includes using a trim mask.

15. The method according to claim 12, wherein said second sidewall comprises a substantially vertical sidewall.

16. The method according to claim 12, wherein said step of simultaneously removing polysilicon comprises simultaneously isotropically etching said polysilicon on the first sidewall.

17. The method according to claim 12, wherein said step of forming the first sidewall with a first slope angle comprises forming said first slope angle to be substantially within a range of about 45 to 65 degrees with respect to a surface of said substrate on which said first sidewall is formed.

18. The method according to claim 12, wherein said step of forming the polysilicon spacer as the floating gate includes forming a notch in said second sidewall between said floating gate and an adjacent floating gate of said memory.

19. The method according to claim 18, wherein said step of forming the

notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on at least two sides thereof.

20. The method according to claim 19, wherein said step of forming the notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on three sides thereof.

21. The method according to claim 13, wherein said step of forming the polysilicon spacer as the floating gate includes forming a notch in said second sidewall between said floating gate and an adjacent floating gate of said memory.

22. The method according to claim 21, wherein said step of forming the notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on at least two sides thereof.

23. The method according to claim 22, wherein said step of forming the notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on three sides thereof.

24. The method according to claim 14, wherein said step of forming the polysilicon spacer as the floating gate includes forming a notch in said second sidewall between said floating gate and an adjacent floating gate of said memory.

25. The method according to claim 24, wherein said step of forming the

notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on at least two sides thereof.

26. The method according to claim 25, wherein said step of forming the notch in said second sidewall between said floating gate and an adjacent floating gate of said memory comprises forming said notch to surround said floating gate on three sides thereof.

27. The method according to claim 14, wherein said step of forming the polysilicon spacer as the floating gate including using a trim mask includes:

depositing a photoresist trim mask to protect an area of the floating gate and removing polysilicon sidewall floating gate material outside the photoresist trim mask.

28. The method according to claim 27, wherein said step of forming the wordline and the floating gate including using a trim mask further includes:

removing the photoresist trim mask; and

depositing and planarizing a dielectric layer over said wordline, said floating gate, and said substrate.

29. The method according to claim 28, wherein, prior to said step of depositing and planarizing said dielectric layer, said step of forming the polysilicon spacer as the floating gate including using a trim mask further comprises:

performing a source and drain implantation, and forming dielectric sidewall spacers on the wordline, and forming source and drain implants and diffusion to form source/drain junctions, and

wherein, after said depositing and planarizing said dielectric layer, said step of forming the polysilicon spacer as the floating gate including

using a trim mask further includes:

opening a contact hole in the dielectric layer to the drain and filling the contact hole with metal; and

depositing and patterning a metal layer over said dielectric layer and said contact hole, to form a bitline,

wherein said metal includes chemical vapor deposition (CVD) tungsten, and said metal layer is formed of any of aluminium, tungsten, silicide, and alloys thereof, and is deposited in a thickness substantially within a range of about 50 nm to 150 nm.

30. The method according to claim 28, wherein said dielectric layer has a thickness substantially within a range of about 50 nm to about 300 nm.

31. The method according to claim 27, wherein said step of forming the polysilicon spacer as the floating gate including using a trim mask further includes:

removing the photoresist trim mask; and

depositing a dielectric layer over said wordline, said floating gate, and said substrate, without planarizing said dielectric layer.

32. The method according to claim 31, wherein said step of forming the polysilicon spacer as the floating gate including using a trim mask further includes:

opening a contact hole in the dielectric layer to the drain and filling the contact hole with metal; and

depositing and patterning a metal layer over said dielectric layer and said contact hole, to form a bitline.

33. The method according to claim 32, wherein said metal includes chemical vapor deposition (CVD) tungsten, and wherein said metal layer is

formed of any of aluminium, tungsten, silicide, and alloys thereof, and said metal layer is deposited in a thickness substantially within a range of about 50 nm to 200 nm,

wherein said step of patterning the bitline comprises etching the metal layer, the dielectric layer to a nitride cap on said wordline such that said wordline is protected, said step of using the trim mask further comprising:

etching the polysilicon spacer to remove unwanted, spacer material, wherein an active area of the device is narrower than the bitline, such that the source/drain is self-aligned to the floating gate.

34. The method according to claim 31, wherein said dielectric layer has a thickness substantially less than about 50 nm.

35. A method of forming a flash memory having a plurality of cells, comprising steps of:

forming a metal-oxide-semiconductor (MOS) transistor including a control gate, such that at least a first side of the control gate has a plurality of notches; and

forming respective floating gates in said notches such that each floating gate is surrounded on a plurality of sides by said control gate.

36. The method according to claim 35, wherein said step of forming said MOS transistor comprises:

forming device isolations in a substrate;

forming a buried interconnect adjacent the isolations;

forming a gate oxide over said substrate and said isolations;

forming a gate stack over said gate oxide, with a doped gate polysilicon being formed on said gate oxide with a nitride cap thereover; and

patterning said gate by lithography and reactive ion etching (RIE).

37. The method according to claim 36, wherein said step of forming said MOS transistor further comprises:

removing the gate oxide exposed in a predetermined area by one of wet etching and dry etching;

depositing a chemical vapor deposition (CVD) nitride layer over said gate stack, and oxidizing said nitride layer, so that a thin layer of oxide is formed underneath the nitride layer and such that a composite oxide/nitride layer is formed on the substrate, as well as at the sidewall of the control gate;

depositing and etching-back a first layer of doped CVD polysilicon, to form sidewall spacers on both sides of the control gate, and such that the nitride layer is removed, and the thin oxide layer remains as a tunneling oxide layer for a second portion of the floating gate;

depositing and etching-back a second polysilicon layer to form a second sidewall spacer, on both sides of the gate stack.

38. The method according to claim 35, further comprising:

trimming said floating gate, said trimming step comprising applying a resist pattern over said floating gate and removing unwanted floating gate material using an existing cap nitride as a mask to protect the control gate.

39. The method according to claim 38, wherein said step of trimming said floating gate comprises:

using the resist pattern as a trim mask to protect the floating gate area, and removing the polysilicon sidewall floating gate outside the trim mask;

removing the resist pattern;

depositing and planarizing a dielectric layer over said floating gate;

forming a contact hole in said dielectric layer to the drain of the

device, and filling said contact hole with metal; and

depositing a metal layer over said dielectric layer and said contact hole, and patterning said metal layer to form a bitline.

40. The method according to claim 38, wherein said step of trimming said floating gate comprises:

using the resist pattern to protect the floating gate area, and removing unwanted polysilicon spacers outside the resist pattern, wherein the resist pattern protects the polysilicon sidewall floating gate on the first side of the control gate with said notches;

removing the resist pattern;

forming an oxide sidewall on the first side of said control gate, and forming source/drain junctions;

leaving remaining polysilicon sidewall floating gate material in the notches;

depositing a dielectric layer over said control gate, without planarizing said dielectric layer;

forming a contact hole in said dielectric layer to the drain of the device, and filling said contact hole with metal; and

depositing a metal layer over said dielectric layer and said contact hole, and patterning said metal layer to form a bitline.

41. The method according to claim 40, wherein said step of patterning said metal layer includes patterning said bit line by first etching the metal layer, and then etching the dielectric layer to a cap nitride, such that the control gate is protected,

said method further comprising:

etching said floating gate to remove unwanted, floating gate material, such that an active area is narrower than the bitline, and such that the source/drain of the device is self-aligned to the floating gate.

42. A method of forming a flash memory, comprising steps of:

forming a silicon substrate with well and isolation structures;

forming, on said silicon substrate, a gate conductor having first and second sidewalls;

forming a notch in one of the first and second sidewalls of the gate conductor for surrounding at least two sides of a floating gate to be formed inside the notch;

forming an insulating layer over the gate conductor;

depositing polysilicon over the insulating layer, and directionally etching the polysilicon, to form a polysilicon spacer;

trimming the polysilicon spacer, to leave the polysilicon spacer inside the notch and just extending over edges of the notch, the polysilicon spacer forming the floating gate; and

forming a dielectric layer over the substrate, the floating gate and the gate conductor, and forming a metal layer over said dielectric layer and connected to a drain formed in said silicon substrate.

43. The method according to claim 42, wherein said substrate includes an implanted n^+ diffusion region, said n^+ diffusion region being for the source connection of the cells of said flash memory.

44. The method according to claim 42, wherein said step of trimming the polysilicon spacer is performed with a trim mask.

45. A method of forming a memory having a plurality of cells, comprising steps of:

forming a substrate with well and isolation structures;

forming a gate oxide over said substrate;

depositing a polysilicon gate material on said gate oxide, to form a

control gate, said control gate including a first sidewall having a first slope angle with respect to said substrate, and a second sidewall having a second slope angle greater than said first slope angle;

selectively removing the gate oxide in an exposed area, and depositing a gate dielectric;

performing a thermal oxidation such that at an interface of said gate dielectric, and at an interface of the polysilicon gate material and said substrate, such that an oxide layer is grown;

forming a sidewall floating gate on the first sidewall such that at least two sides of the sidewall floating gate are surrounded by said first sidewall; and

forming a tunneling region underneath the floating gate.

46. The method according to claim 45, wherein said first sidewall is tapered and said second sidewall is substantially vertical with respect to the substrate,

wherein said step of forming a sidewall floating gate includes using a phase shift mask comprising phase shift regions for producing a tapered shape and an opaque mask without phase shift modifications for producing the substantially vertical second sidewall.

47. The method according to claim 45, wherein said first sidewall is tapered and said second sidewall is substantially vertical with respect to the substrate,

wherein said step of forming a sidewall floating gate includes using a trim mask for trimming unwanted polysilicon gate material outside an area of the sidewall floating gate.

48. The method according to claim 45, wherein said step of forming the sidewall floating gate includes forming the sidewall floating gate in a notch

formed in said second sidewall, the notch surrounding said at least two sides of the sidewall floating gate.

49. The method according to claim 48, wherein said notch surrounds three sides of the sidewall floating gate.